An integrated capacitance bridge for high-resolution, wide temperature range quantum capacitance measurements

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We have developed a highly-sensitive integrated capacitance bridge for quantum capacitance measurements. Our bridge, based on a GaAs HEMT amplifier, delivers attofarad (aF) resolution using a small AC excitation at or below k_BT over a broad temperature range (4K-300K). We have achieved a resolution at room temperature of $10\text{aF}/\sqrt{\text{Hz}}$ for a 10mV AC excitation at 17.5 kHz, with improved resolution at cryogenic temperatures, for the same excitation amplitude. We demonstrate the performance of our capacitance bridge by measuring the quantum capacitance of top-gated graphene devices and comparing against results obtained with the highest resolution commercially-available capacitance measurement bridge. Under identical test conditions, our bridge exceeds the resolution of the commercial tool by up to several orders of magnitude.

I. INTRODUCTION

As device scaling continues below 20 nm and novel nanodevices appear on the horizon, accurate characterization and detailed understanding of their electronic structure is essential, yet challenging[1]. For example, carrier transport through a nanostructure, which is often quantified by mobility, cannot be accurately characterized from conductance alone without knowing the exact carrier density. Information on carrier density is often extracted from a capacitance spectrum by measuring the capacitance between the device channel and a gating terminal as a function of DC bias, commonly known as a CV curve.

In most field-effect semiconductor devices, a dielectric layer isolates the channel from the gate electrode. The capacitance measured from the gate is the series combination of the geometric capacitance associated with the dielectric, C_{ox}, and the capacitance associated with adding carriers to the bandstructure of the semiconductor, or the quantum capacitance, C_Q, which is proportional to the electronic density of states (DOS)[2–4]. For devices with large DOS in the channel, the effective gate capacitance is simply the geometric capacitance C_{ox}. However, in nanoscale devices with strongly coupled gates, a low DOS in the channel can reduce the quantum capacitance to hundreds of attofarads, making C_Q dominate the total gate capacitance. In this regime, the total capacitance is a strong function of the channel DOS. In order to fully resolve fine bandstructure features, for example van Hove singularities in carbon nanotubes[5], an external excitation smaller than the characteristic thermal energy k_BT is necessary. Inevitably, any practical measurement setup will include some length of cables that have a finite parasitic capacitance on the order of hundreds of picofarads. This produces an enormous attenuation of the test signal, pushing even state-of-the-art laboratory CV meters beyond their resolution limits when such small test signals are used, as illustrated in Fig. 1a.

In this work, we present an integrated capacitance bridge to extract and balance the test signal coming from a nanostructure before it is attenuated by external cables. We demonstrate excellent capacitance resolution for test signals less than k_BT from room temperature down to temperatures of 4K, yielding an output noise of less than $10\text{nV}/\sqrt{\text{Hz}}$. We compare our device to a commercially available, state-of-the-art capacitance/loss measurement tool, and are able to significantly exceed its performance when measuring the capacitance of top-gated graphene devices.

II. BRIDGE DESIGN AND OPERATION

The principles of operation of the capacitance bridge are explained by Steele *et al.*[6] The bridge consists of a reference impedance and an impedance-matching amplifier, whose function is to drive the large parasitic cable capacitance and isolate the device under test (DUT). Since we are interested in measurements across a broad temperature range down to cryogenic temperatures, we use a GaAs-based high electron mobility transistor (HEMT) as the impedance-matching amplifier[7]. A standard Si FET is unsuitable due to carrier freeze-out at low temperature. The HEMT in our bridge is an unpackaged FHX35X transistor manufactured by the Fujitsu Corp, and has a wide ($\sim 280\mu$m) channel fabricated from epitaxially-grown GaAs, with a gate capacitance $\sim$0.4pF[8]. The 2D electron gas is fully depleted when the gate is biased at -1V (depletion mode).

The reference impedance is used to balance the signal across the DUT, and its AC impedance must be larger than the HEMT gate AC impedance to avoid shunting of the DUT signal. As the HEMT gate is DC biased through the reference (via a Yokogawa 7651 pro-

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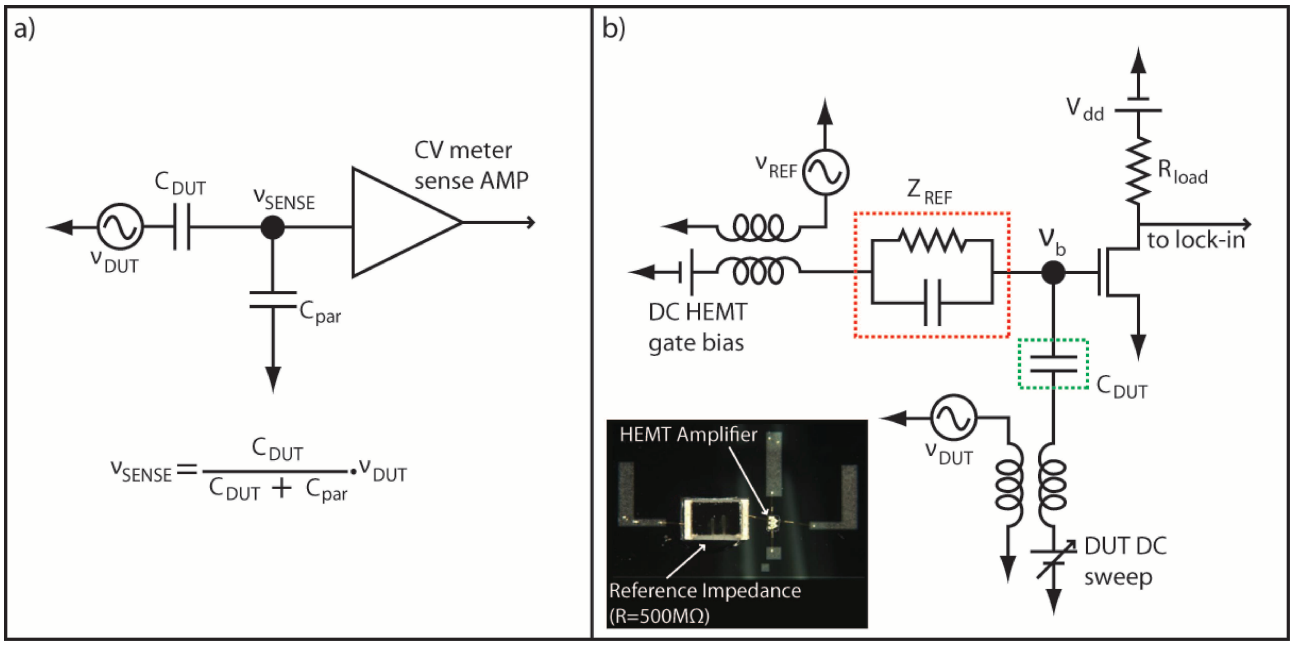

FIG. 1. a) Parasitic cable capacitance in a typical capacitance test setup with a CV meter. For small C_{DUT}, the test signal ν_{DUT} is attenuated by a factor of $\sim C_{DUT}/C_{par}$, which is on the order of 10^6 for typical nanostructures connected via standard coaxial cables. For $\nu_{DUT} \sim k_B T$ at 4K, this results in $\nu_{sense} < 1$nV. b) Schematics of our bridge circuit connected to a DUT. AC and DC signals are added together with a Triad Magnetics SP-67 audio transformer. The inset contains a photograph of the bridge on the GaAs substrate before wirebonding to the DUT.

grammable low-noise DC power supply), the reference DC impedance should ideally be at most of the same order as the HEMT gate resistance across all temperatures. To satisfy these constraints at the test frequency 17.5 kHz, we use a 500 MΩ thick-film resistor (Tyco Electronics part no. 26M2248) with a low thermal coefficient and a parasitic capacitance $C_{REF} \sim 110$fF. A 1kΩ load resistor (Vishay Dale no. CCF551K00FKE36) is used to bias the HEMT drain. Bridge schematics and a photograph are shown in Fig. 1b.

To avoid strain and thermal gradients at low temperature, a thermally-matched substrate is required to mount the bridge circuit. We used a semi-insulating GaAs wafer as the substrate, onto which a 23nm Al_2O_3 layer was grown via ALD for additional electrical isolation. Standard photolithography/liftoff processing were used to fabricate 300nm thick Al electrodes for bonding. The bridge components were then attached to the substrate, using thermally-conductive silver epoxy for the HEMT and PMMA for the reference resistor, then wirebonded to the pads.

In operation, two out-of-phase AC signals, ν_{DUT} and ν_{REF}, are simultaneously applied to the DUT and reference resistor, respectively. The signal ν_b at the so-called "bridge point" is then given by

$$\nu_b = \frac{Y_{DUT}}{Y_\Sigma}\nu_{DUT} + \frac{Y_{REF}}{Y_\Sigma}\nu_{REF}, \qquad (1)$$

where Y refers to the AC admittance and $Y_\Sigma = Y_{DUT} + Y_{par} + Y_{REF}$ is the total admittance seen from the bridge

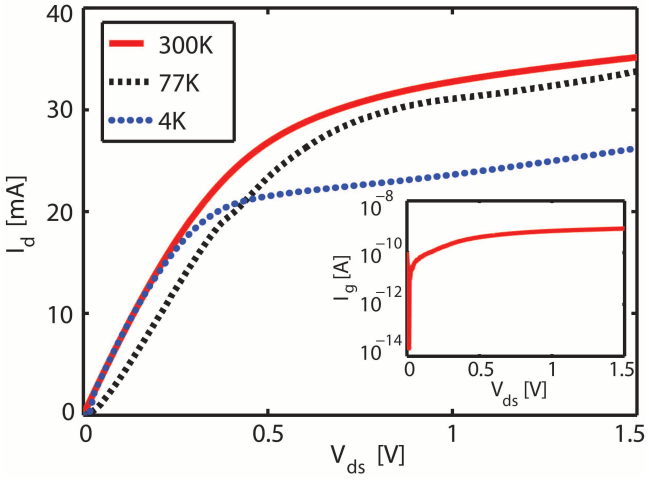

FIG. 2. Output characteristics of Fujitsu FHX35X HEMT for $V_{gs} = 0$ at various temperatures. The inset shows the gate current I_g as a function of V_{ds} for $V_{gs} = 0$ (no load resistor). For temperatures 77K and below, the leakage is below 1pA.

point. The "par" subscript refers to parasitic terms, including the HEMT gate impedance. When balanced, i.e. $\nu_b = 0$, the amplitude and phase of the DUT impedance are given by

$$Z_{DUT} = \frac{-\nu_{DUT}}{Y_{REF} \cdot \nu_{REF}}, \qquad (2)$$

independent of any parasitic capacitances. Output char-

TABLE I. Optimized HEMT bias conditions with corresponding amplifier output sensitivity S and best achievable capacitance resolution $\delta\tilde{C}$ (measured using C_{DUT}=250aF, before bonding graphene device to bridge).

T[K]	V_{dd}[V]	V_{gs}[mV]	S[nV/$\sqrt{\text{Hz}}$]	HEMT Gain	$\delta\tilde{C}$ (ν_{DUT} =10mV rms) [aF/$\sqrt{\text{Hz}}$]
300	4	-50	8	0.05	9.6
77	4	-50	7.4	0.063	7
4.2	4	-25	5.6	0.1	3.4

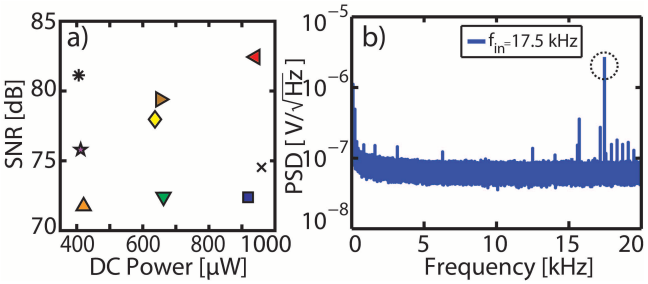

FIG. 3. a) Integrated bridge output SNR as a function of DC power dissipation for a 1.5mV RMS input signal at room temperature. The symbols in the plot correspond to the following $(V_{gs}[V], V_{dd}[V])$ pairs: $*$ (-0.05,4), ★ (-0.1,4), ▲ (-0.15,4), ▶ (-0.1,5), ♦ (-0.05,5), ▼ (-0.15,5), ◀ (-0.1,6), × (-0.15,6), ■ (-0.05,6). The optimal bias point, i.e. high SNR and low power, is marked by $*$. b) output power spectral density (PSD) of the bridge (measured with a home-built spectrum analyzer) biased at the optimal bias point(-60 dB gain between bridge input and output) with 100μV RMS input signal). The excitation at 17.5kHz is indicated by the black circle.

acteristics and gate leakage[9] (below 1 nA) of the HEMT are shown in Fig.2. The bias point for the HEMT is chosen to maximize SNR while keeping the DC power as low as possible to avoid thermal drift and temperature gradients during measurement[10]. We found that the optimal bias point for the HEMT is in the triode regime, which has low gain, but also very low noise and thermal drift. Fig.3 shows SNR and DC power dissipation for the HEMT as a function of V_{gs} and V_{dd} applied to the 1kΩ load resistor R_{load}, as well as the output power spectrum for the optimal bias point at room temperature for an RMS input AC excitation of 1.5mV at 17.5 kHz. The spectrum is flat except for low frequencies (below 1kHz), where $1/f$ noise dominates. We use a Stanford Research Systems lock-in amplifier (model SR830) to recover the small AC output of the amplifier. We define the output sensitivity $S = \Delta n\sqrt{t_{meas}}$, where Δn is the RMS noise in the measured data points sampled with the lock-in, and t_{meas} is the lock-in measurement time[11] per data point. At each temperature, we perform a HEMT bias optimization prior to the capacitance measurement. The optimal bias points with corresponding output sensitivity S for a range of temperatures are given in Table I. The sensitivity improves only slightly with temperature, as the bridge performance is limited by $1/f$ noise from the HEMT.

III. EXPERIMENTAL SETUP AND MEASUREMENTS

To demonstrate the performance of our bridge, we compare it against the popular Andeen-Hagerling model 2700A precision capacitance and loss measurement bridge, the highest resolution CV meter commercially available. The performance of the commercial bridge was first quantified by measuring a standard shielded 9.3pF capacitor[12]. As expected, the measured sensitivity is a strong function of the test signal (∼200 and ∼80aF/$\sqrt{Hz}$ for 100mV and 250mV rms test signals, respectively, in good agreement with the manufacturer specification). Based on these measurements, more than 10 hours of averaging per data point would be required to obtain 1 attofarad resolution for a 100mV test signal, which still has a peak-to-peak amplitude of more than $10k_BT$ at room temperature. However, we can avoid long measurement averaging times for the comparison between our bridge and the commercial bridge by measuring the capacitance of graphene devices with strongly-coupled top gates, as the quantum capacitance of such structures can easily be resolved by the commercial bridge.

The graphene in our device was deposited on a SiO_2/Si chip via mechanical exfoliation, and confirmed to be single-layer via optical contrast and confocal Raman spectroscopy. 100nm of PMMA was spin-coated, and source/drain leads to a selected graphene sheet were defined with e-beam lithography. Following Ti/Au deposition (5/40 nm, respectively) and liftoff in acetone, the entire chip surface was coated via e-beam evaporation with nominally 1.5 nm of Al, which then oxidized almost immediately upon exposure to air. A top-gate electrode was patterned on top of the graphene by e-beam lithography, followed by 40nm of e-beam evaporation of Al and liftoff in acetone[13,14]. An AFM image of the device is shown in the inset of Fig. 4. The graphene device chip was finally wirebonded to the bridge chip, and both chips were mounted on a copper support for thermal anchoring.

Measurements were carried out in a Lakeshore/Desert Cryogenics variable temperature probe station. The HEMT gate impedance Z_{gate} was characterized by measuring the difference in HEMT response between exciting the HEMT gate directly through its small bond pad and exciting the gate through the reference impedance. The signal attenuation G is then related to the impedances by the equation $G = \frac{Z_{gate}}{Z_{gate}+Z_{REF}}$. These complex impedance values are used to calculate the relative phase between ν_{REF} and ν_{DUT} required to for balancing the

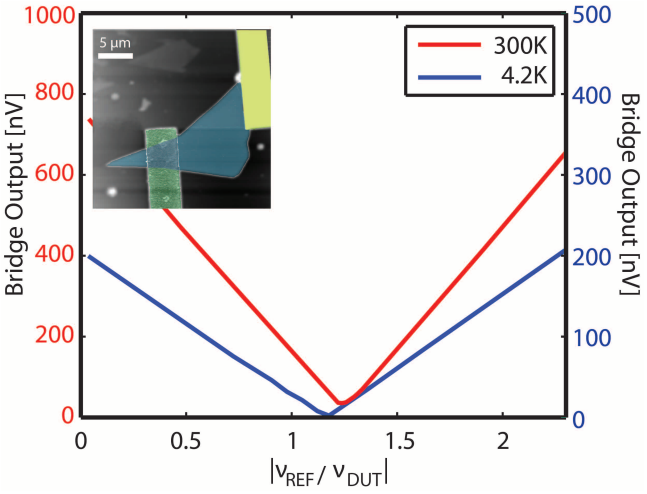

FIG. 4. Integrated bridge output as a function of $|\nu_{REF}/\nu_{DUT}|$ for T=300K (left axis), with ν_{DUT}=8mV and phase difference between graphene DUT and REF signals $\Delta\Phi$=144°; and for T=4.2K (right axis), with ν_{DUT}=100μV and $\Delta\Phi$=155°. The bridge output minimum and phase difference $\Delta\Phi$ are shifted slightly between the two curves due to changes in the REF and DUT impedances with temperature. The inset shows a false-color AFM image of the measured graphene device. The graphene is colored blue, the source/drain contact is gold, and the top-gate is colored green.

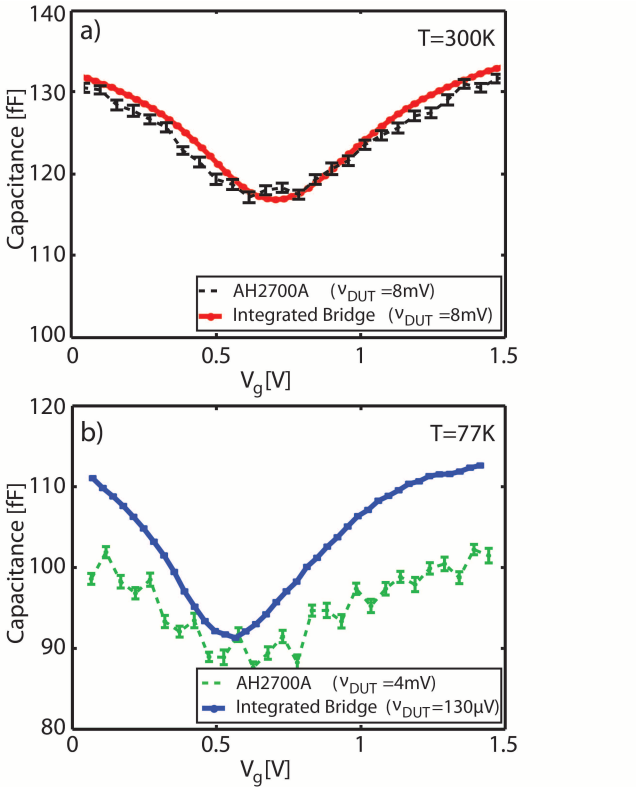

FIG. 5. CV curves for top-gated graphene device for both the AH2700A and the integrated bridge. Acquisition time for all measurements was held constant (~30s per point) to enable direct comparisons between measurements[16]. a) At room temperature using an 8mV DUT excitation, noise in the integrated bridge measurement is ~11aF, while the noise for the commercial bridge is ~675aF. b)At 77K, the smallest possible DUT excitation of 4mV was used for the commercial bridge measurement, and the Dirac point is poorly resolved due to the high noise level~5000aF. For the integrated bridge measurement, the Dirac point is cleanly resolved while using a small DUT excitation of 130μV, with a noise level~53aF.

bridge. Bridge balance curves are shown in Fig.4. The change in capacitance of the graphene as the top-gate DC bias is swept (also via Yokogawa 7651) is then calculated from the change in bridge signal ν_b using (1).

Capacitance from bond pads, wirebonds, and probe tips contribute to the parasitic capacitance C_{par}, which is in parallel with C_{DUT} and sets the baseline of the measurement. The parasitic capacitance remains constant throughout the measurement and is often larger than the change in device capacitance caused by the modulation of carrier density inside the device as a function of gate bias. We define the measurement sensitivity[15] $S_{meas} \equiv \left|\frac{\partial \nu_b}{\partial Y_{DUT}}\right|$, so that we have:

$$\delta C_{DUT} \sim \delta Y_{DUT} = \frac{1}{S_{meas}} \delta \nu_b. \quad (3)$$

Evaluating the derivative in (4) using (1), we find the expression for the sensitivity:

$$S_{meas} = \left| \frac{(\nu_{DUT} - \nu_{REF}) Y_{REF} + \nu_{DUT} Y_{par}}{(Y_{DUT} + Y_{REF} + Y_{par})^2} \right| \quad (4)$$

Thus, the measurement sensitivity is maximized by increasing ν_{DUT}. However, in practice, we limit this excitation to $\nu_{DUT} \sim k_B T$ to prevent thermal drift and heating, and to avoid blurring of density-of-states features by our excitation.

IV. RESULTS AND DISCUSSION

2D Graphene has no energy gap between the conduction and valence bands. Instead, these bands meet at a point, termed the Dirac point, about which the energy-momentum dispersion is linear. The density of states and associated quantum capacitance C_Q therefore vary linearly with energy near the Dirac point. As the top-gate bias voltage is swept, the Fermi level scans the graphene energy spectrum, passing through the Dirac point, where the capacitance reaches a minimum[17]. For top-gate voltages that tune the Fermi level far in energy from the Dirac point, the density of states and associated C_Q are large, so that C_{ox} will dominate.

Fig. 5a,b show graphene capacitance measurements for both our integrated bridge and the AH2700A at room temperature and 77K, respectively. The capacitance is symmetric about the Dirac point, which occurs at a top

gate voltage V_g ∼1V. At room temperature, with an AC excitation of 8mV for ν_{DUT}, the overall capacitance curves match for the two measurements[16], though our integrated bridge is significantly less noisy (δC for integrated bridge is ∼11aF; for AH2700A, δC ∼675aF). At 77K, the minimum allowable excitation amplitude of 4mV was used for ν_{DUT} for the AH2700A measurements (peak-to-peak amplitude∼ $2k_BT$), while a substantially lower excitation of 130μV was used for ν_{DUT} for the integrated bridge measurements (peak-to-peak amplitude∼ $k_BT/18$). The capacitance curve is again cleanly resolved for the integrated bridge measurements (δC ∼53aF), with improvement in the sharpness of the capacitance around the Dirac point due to lower temperature and excitation (depth of Dirac point capacitance dip ΔC increased from ∼15fF to ∼21fF), whereas these features are obscured by the excessive noise level for the AH2700A measurements (δC ∼5000aF).

V. CONCLUSIONS

We have demonstrated a reliable method for integrated high-resolution quantum capacitance measurements over a wide temperature range using an integrated bridge circuit directly wirebonded to the DUT. The performance of our bridge was tested against the commercially available AH2700A capacitance bridge by measuring the capacitance of a top-gated graphene device. We observed significant resolution improvements over the commercial tool, enabling the fast measurement of quantum capacitance for nanostructures down to cryogenic temperatures, and achieving 10s of attofarad resolution per root hertz at room temperature (equivalently, less than 1 e^- per root hertz on the DUT) while limiting the excitation amplitude to below k_BT.

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[8] Several other commercially available HEMTs, including the Agilent ATF 33143 and 34143, were found to be unsuitable in our measurements due to high-frequency (MHz) transport resonances.

[9] Measured via an Agilent B1500A parameter analyzer and Keithley 2612.

[10] All measurements were performed in the dark to prevent optical excitation of the exposed 2DEG in the HEMT. After cooling, HEMTs were temporarily exposed to light, to enable navigating probes to pads, so persistent photoconductivity may affect HEMT characteristics at 77K and 4K.

[11] Measurement time t_{meas} is proportional to the lock-in time constant and filter slope (SRS830 manual).

[12] The standard capacitor was measured using two different AH2700A units in two separate locations.

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[15] The signal-to-noise ratio is related to the measurement sensitivity by $SNR = S_{meas}\frac{Y_{DUT}}{\nu_b}$.

[16] The acquisition time for each data point (∼30s) is approximately equal for both the integrated bridge and the AH2700A measurements, allowing for direct comparison between curves. Note that this per-point acquisition time contains settling times as well as wait times associated with polling the GPIB bus.

[17] The minimum capacitance is limited by the temperature, disorder, and parasitic capacitance[13].